REMARKS

This divisional application is being filed due to an election requirement contained in the Office Action dated 11/06/2003, in parent application serial no. 10/094,161.

The pending claims are directed to a method for fabricating semiconductor components 16A (Figure 8F) or 16PGA (Figure 19G). As shown in Figure 8A, the method includes the step of providing a plurality of semiconductor dice 14A on a substrate 12A. As shown in Figure 8B, the method also includes the step of forming conductive vias 68A in the dice 14A, and trenches 28A in the substrate 12A along the peripheral edges of the dice 14A. In addition, the conductive vias 68A can include contact bumps 24A.

As shown in Figure 8C, the method also includes the step of forming polymer filled trenches 28AP by depositing a polymer layer 36A on the substrate 12A and in the trenches 28A. As shown in Figure 8D, the method also includes the step of thinning the substrate 12A from the back side to the polymer filled trenches 28AP. As shown in Figure 8E, the method also includes the step of forming a back side polymer layer 38AP, and terminal contacts 42A on the conductive vias 68A. As shown in Figure 8F, the method also includes the step of forming grooves 44A through the polymer filled trenches 28AP to singulate the dice 14A.

As shown in Figure 19D, the method can also include the step of etching the substrate 12T-PGA exposing tip portions of the conductive vias 68PGA and forming pins 77PGA. As shown in Figure 19E, the method can also include the step of forming non-oxidizing layers 79PGA on the pins 77PGA. In this case the pins 77PGA function as terminal contacts for the component 16PGA.

Also being submitted in the present application is an Information Disclosure Statement. Should any issues arise that will advance this case to allowance, the Examiner is asked to contact the undersigned by telephone.

DATED this 21st of November, 2003.

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Date of Deposit: November 21, 2003

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November 21, 2003
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